SILICON LDMOS POWER TRANSISTOR

7 W, up to 1000 MHz, Enhancement Mode

The silicon LDMOS transistor die is designed for large-signal output and driver stages up to 860 MHz frequency range. This transistor is typically used for construction of terminal cascades of power amplifiers or transmitter applications.

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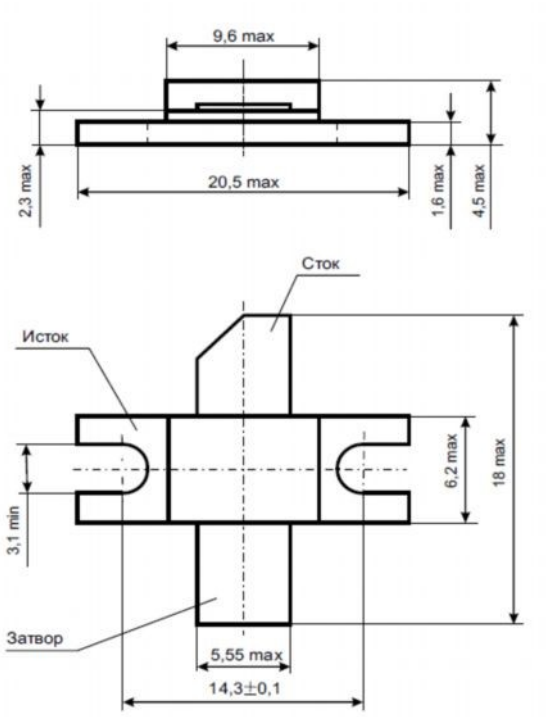
Features:

- Performance at 860 MHz, 28 Vdc
- Power Gain: 11 dB Min
- Output Power: 7 W
- Efficiency: 40 % Min



Case KT-55C-1

Absolute Maximum Ratings

Parameters	Sym	Value	Unit
Drain-Source Voltage	V_{DSS}	60	V_{DC}
Drain Current-Continuous	I_D	1.5	A_{DC}
Gate-Source Voltage	V_{GS}	±20	V_{DC}
Storage Temperature Range	T_{STG}	-65 tu +150	ºC
Thermal Resistance, Junction to Case	R_{qJC}	10	ºC/W
Total Power Dissipation @T_C=25 ^oC	P_D	17.5	W

Parameters

Parameter	Symbol	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage (I_D=10 mA, V_{GS}=0 V)	$V_{(BR)DSS}$	60	—	—	V_{DC}
Gate-Source Leakage Current (V_{GS}=20 V, V_{DS}=0 V)	I_{GSS}	—	—	1.0	mA_{DC}
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 V, V_{GS}=0 V)	I_{DSS}	—	—	2.0	mA_{DC}
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 20 mA)	$V_{GS(TH)}$	1	—	5	V_{DC}
Forward Transconductance (V_{DS} = 10 V, I_D = 0.3 A)	G_{FS}	0.3	—	—	mhos
Input Capacitance (V_{DS} = 28 V, V_{GS}=0 V, f = 1 MHz)	C_{ISS}	—	22	—	pF
Output Capacitance (V_{DS} = 28 V, V_{GS}=0 V, f = 1 MHz)	C_{OSS}	—	11	—	pF
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS}=0 V, f = 1 MHz)	C_{RSS}	—	2.2	—	pF
Power Gain (V_{DS} = 28 V, P_{OUT} = 5 W, $I_{DQ.}$ = 50 mA, f = 500 MHz)	Gp	11	14	—	dB
Drain Efficiency (V_{DS} = 28 V, P_{OUT} = 5 W, $I_{DQ.}$ = 50 mA, f = 500 MHz)	h_D	40	50	—	%

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